Circuit Breaker Type-A SW Design Specification

# Modules Design.

## System Clocking

Use internal low frequency clock 32.768K as FLL input, set core clock to 96MHz.

Since internal clock source is not accurate, auto-trim must be done.

ATM (Auto TRIM Machine) in MCU is used to trim the internal 32K with external 8MHz crystal oscillator. This trim procedure is done at very beginning of main program.

## AD Converter Mechanism

Use ADC0, 16-bit single ended, SW trigger mode. No DMA. Enable interrupt.

Use FTM0 as timer, overflow period 500uS. Enable interrupt.

When FTM0 ISR triggered, it sends notification to task vADC, vADC then trigger AD conversion on 1st channel and wait for the notification of AD conversion complete.

When 1st channel AD conversion completed, ISR triggered and send notification to vADC.

vADC then get the result and starts AD conversion on 2nd channel, and so on.

When all 3 channels are measured, task vADC stored 3-phase AD results to buffer for further use.

## Debug Console Output

Use SDK component fsl\_debug\_console for outputting information via UART1.

Debug\_printf() function using polling mechanism, so CPU will simply wait until all characters transmitted.